A Hybrid MMC Control Strategy to Enhance the Resilience of DC Transmission System

Jun Mei, *Member, IEEE*, Jiawei Guo, Weiye Diao, *Student Member, IEEE*, Renfei Wo, Linyuan Wang, Ao Liu, and Guanghua Wang

***Abstract*—Offshore wind power through flexible dc transmission system faces the challenge of comprehensively improving the transient and steady-state performance. However, existing control strategies often fail to address both simultaneously. This article proposes a coordinated control strategy based on the hybrid modular multilevel converter that can enhance the transient and steady-state resilience of the flexible dc transmission system. First, the coupling relationship between the submodule capacitor voltage and active power is analyzed, and submodule virtual capacitance control (SVCC) is proposed to enhances the dc inertia. Second, the rate of change of dc current is introduced into the dc control loop. The virtual inductance control (VIC) is proposed, which can actively limit the rate of rise of dc current at the initial stage of dc fault. The link of the hysteresis comparator is designed to avoid frequent misoperation of VIC control caused by dc voltage disturbance. At the same time, the positive adjustment capability of the SVCC is used to reduce the fluctuation of the capacitor voltage during the dc fault ride-through process, avoid the switching of the working mode of the ac loop controller, and realize the cooperative control of the transient and steady-state performance. Finally, the effectiveness of the proposed control strategy is verified through simulations and experiment.**

***Index Terms*—Hybrid modular multilevel converter (HMMC), resilience, transient and steady-state performance, virtual capacitance, virtual inductance.**

I. Introduction

THE modular multilevel converter (MMC) is a crucial component of offshore wind power transmission through flexible dc transmission systems. Due to its ability to transmit large amounts of power over long distances with minimal energy loss, it is the optimal solution for high-power transmission in deep and distant seas [1], [2]. Presently, there are several demonstration projects in operation, including the ±320 kV flexible direct transmission project in the North Sea of Germany and the ±400 kV offshore wind farm in Rudong of China. However, as the use of power electronics becomes more prevalent, the resilience of the flexible direct transmission system faces significant challenges [3].

The resilience of a power system refers to its ability to prepare for and quickly recover from disturbances, adapt to changes, and resist disruptions [3], [4], [5]. In the case of offshore wind power transmission systems, the power electronic-based flexible transmission system based on the PI control of the inner and outer loops exhibits "low inertia and weak damping"[6], [7], [8], [9], [10], which implies low resilience [3]. The fluctuation of renewable energy output and load can cause system voltage fluctuations or instability, posing significant challenges to grid stable operate and hinder the potential support of new energy to supplement the grid. In addition, the low resilience exacerbates the evolution of current during dc faults, which can lead to a series of challenges, such as serious fault overcurrent, difficulty in fault isolation, network self-healing, and difficulty in ensuring power supply reliability. The lack of resilience has become a common problem that affects the steady-state and fault-transient performance of flexible dc system [3], [10], [11]. However, there are certain contradictions and differences between the two in terms of demand objectives, which should be solved collaboratively from several aspects, such as scheme design and control strategy improvement.

To improve the steady-state performance, [12], [13], [14], [15], [16] use the fast regulation speed of power electronics to enhance the inertia level. The authors in [12] and [13] proposed the virtual dc motor control that unifies the damping and inertia of the system. The authors in [14] and [15] modified the damp factor so that it adapts itself to the change in dc voltage to regulate the power interaction of the converter. In [16], the inertia of the dc voltage is enhanced by fitting an equivalent capacitance on the dc side of the system by attaching a virtual inertia control. However, although the above can improve the stability of dc voltage, indiscriminate response to dc voltage changes, when the dc voltage starts to drop due to short-circuit faults, the inertia link will continuously inject energy into the dc system, which in turn worsens the rise of dc fault current and is detrimental to the safe operation of the grid.

In terms of improving transient performance, researchers have proposed various techniques to enhance the dc fault handling

Manuscript received 21 May 2023; revised 17 October 2023; accepted 6 December 2023. Date of publication 1 January 2024; date of current version 5 June 2024. This work was supported by the National Natural Science Foundation of China under Grant 52077037. *(Corresponding author: Jiawei Guo.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIE.2023.3344814.

Digital Object Identifier 10.1109/TIE.2023.3344814

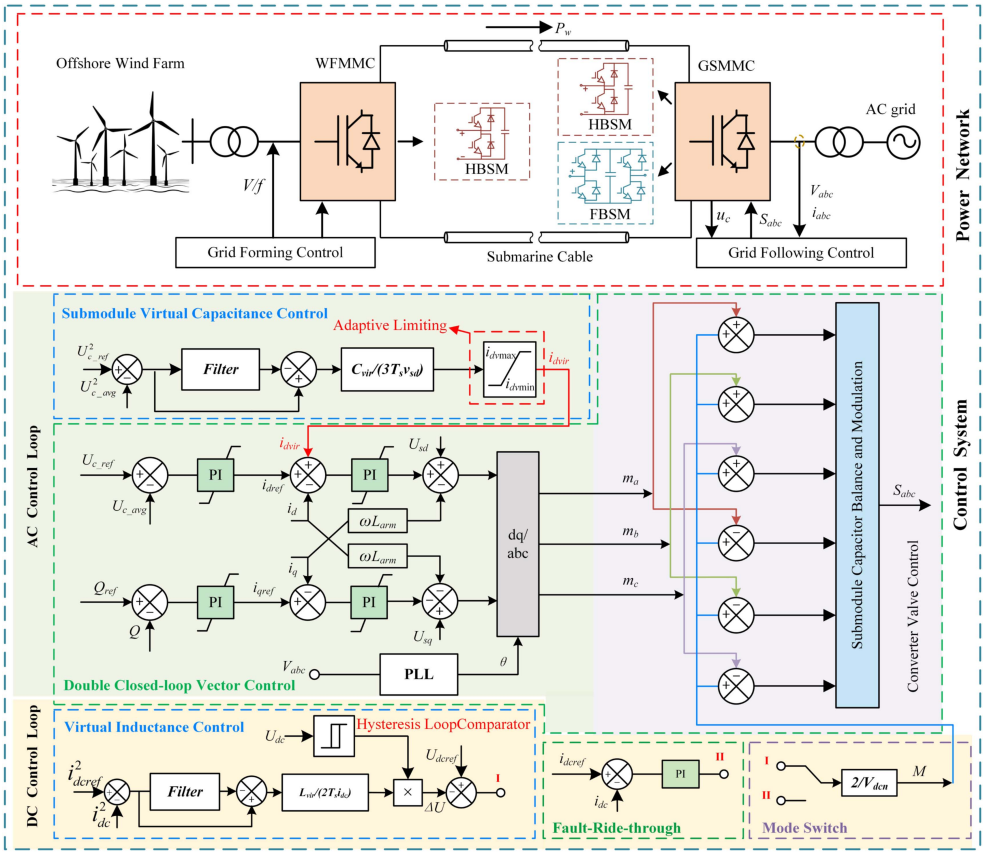


Fig. 1. Topology and control structure of offshore wind power through flexible dc transmission system.

capability of the flexible dc system. The authors in [17] and [18] proposed hybrid MMC (HMMC) consisting of half-bridge submodule (HBSM) and full-bridge submodule (FBSM), which switches to constant current control to complete fault ride-through. However, HMMC relies on the line protection device to send mode-switching signals, and the switching delay can cause the short-circuit current to evolve too quickly and cause the converter station to block. In [19], the effect of mode switching time on the initial dc fault current is analyzed, but the method of suppressing the current at the beginning of the fault is not given in detail. For the initial stage of the fault, the most common method is to utilize dc line upper current reactors [20], [21], but excessive line reactance will not only increase the construction cost, but also affect the stability of the dc system. In [22], the method of using the converter valve to detect fault occurrence was proposed, but the method has poor anti-interference capability, which will seriously threaten the stable operation of the grid if the control loop is misoperated due to sampling errors. The authors in [18] and [23] added the dc voltage as a feedforward quantity to the control at the initial stage of the fault to reduce the current by rapidly reducing the number of submodule (SM) inputs. However, due to the strong coupling between the output quantity and the dc voltage, when the renewable energy power disturbance causes the dc-bus voltage fluctuation, it will make the number of input SMs decrease, which in turn worsens the dc voltage fluctuation.

The above studies reveal that the flexible dc transmission system faces challenges with poor antidisturbance capability under steady-state conditions and weak dc fault handling capability. Although several means of voltage stability enhancement and fault current transient handling techniques exist, they are fragmented and not mutually supportive. The use of virtual inertia control enhances the steady-state performance of the dc system but affects the evolution process of fault currents under transient conditions. Strengthening the coupling relationship between dc voltage and current-limiting control tends to exacerbate dc voltage fluctuations under steady-state conditions. DC system steady-state and transient performances are affected by the performance of the "loss of both" situation.

To overcome the limitations of existing control strategies, this article proposes a control strategy to enhance the resilience of the dc system. The major contributions are as follows.

1) Based on HMMC, the submodule virtual capacitance control (SVCC) is proposed. A larger virtual SM capacitance can be fitted during the disturbance, thereby reducing the fluctuation of the dc voltage.
2) The virtual inductance control (VIC) is proposed. It can fit a larger current-limiting reactance on the dc circuit during a fault, thereby reducing the rise of the fault current.
3) By cooperating the two control methods, the control strategy can optimize the resilience of both steady-state and transient conditions simultaneously.

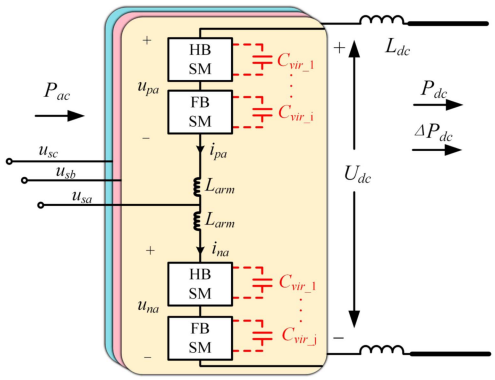


Fig. 2. Hybrid MMC topology.

The rest of this article is organized as follows. In Section II, the hybrid MMC ac–dc decoupling control principle is analyzed. Section III proposes the resilience enhancement strategies. Section IV analyzes the advantages realized by the combination of the two control methods. In Section V, the selection of key parameters is carried out through stability analysis. Sections VI and VII establish the simulation and experimental models to verify the effectiveness of the proposed control strategy. Finally, Section VIII concludes this article.

II. Principle of HMMC AC–DC Decoupling Control

A. Offshore Flexible DC Transmission System

The topology and control of the offshore flexible dc transmission system are shown in Fig. 1. Offshore wind turbines have low capacity and weak stabilizing force, so the wind farm side MMC usually adopts *V/f* control to undertake the function of constructing the offshore ac power grid. The grid side MMC mainly controls the voltage of the direct grid [2]. Considering the limited resources of the offshore platform, there are certain requirements for the volume, weight, and redundant configuration of the converter station. In consideration of economy and fault ride-through requirements, the following research will mainly focus on the grid-side converter, employing grid-following control, and the HMMC. The topology is shown in Fig. 2, where u_{pj}, u_{nj}, i_{pj}, and $i_{nj}(j = a, b, c)$ denote the voltage and current of the upper and lower bridge arms, respectively, u_{sj} indicates the j-phase ac voltage, L_{arm} implies the bridge arm inductance, and L_{dc} represents the dc reactor.

B. Decoupling Principle of HMMC AC–DC System

In Fig. 2, ignoring the voltage drop across the bridge arm reactance, obtained as follows:

$$\begin{cases} u_{pj} = \frac{1}{2}U_{dc} - u_{sj} \\ u_{nj} = \frac{1}{2}U_{dc} + u_{sj} \end{cases}. \tag{1}$$

The bridge arm voltage is composed of the dc component and the ac component. Define dc voltage modulation ratio M. It indicates the number of SMs mapped to the dc side. Thus, $M \le N$, and N is the number of SMs of the half-bridge arm. The function of the valve-side controller makes the capacitor voltage of each SM approximately equal to U_{c_avg}. The above formula simplifies to

$$U_{\text{dc}} = MU_{c\_\text{avg}}. \tag{2}$$

Based on (1) and (2), the control of the HMMC can be decomposed into two parts: ac and dc control loop. Here, the ac control loop controls the power interaction between the hybrid MMC and the ac grid, and the capacitor voltage of all SM in the converter station is maintained at the rated value. When the converter station works in a steady state, $P_{\text{ac}} = P_{\text{dc}}$, and $U_{c\_\text{avg}} = U_{c\_\text{ref}}$. The dc control loop controls the M of SM mapped to the dc side. During normal operation, $M = N$. When a dc fault occurs, the reverse input of the full-bridge SM reduces M rapidly, and U_{dc} also decreases to limit the fault current.

III. Resilience Enhancement Strategy

A. SVCC Strategy

1) Control Principle: When the dc power of the MMC is disturbed, the power relationship evolves as follows:

$$P_{\text{dc}} + \Delta P_{\text{dc}} = P_{\text{ac}} + NP_{c\_\text{avg}} = P_{\text{ac}} + NC_{c0}\frac{\text{d}u_{c\_\text{avg}}}{\text{d}t} \tag{3}$$

where P_{c_avg} and C_{c0} are the average power and capacitance of the SM, respectively. It can be concluded from the above formula that when the dc power is disturbed, the capacitor voltage of the SM will fluctuate accordingly, causing the dc voltage to oscillate. In (3), C_{c0} is embedded in the topology structure and cannot be changed arbitrarily, so the SM virtual capacitance C_{vir} can be introduced from the control to reduce the change of the SM capacitor voltage

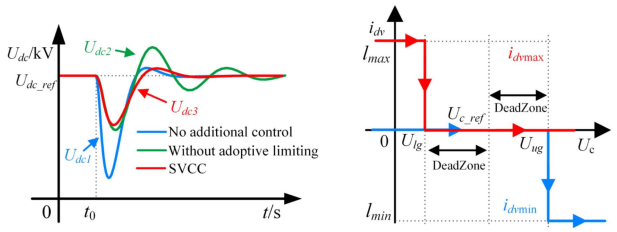
$$\begin{aligned} P_{\text{dc}} + \Delta P_{\text{dc}} &= P_{\text{ac}} + N\left(C_{c0} + C_{\text{vir}}\right)\frac{\text{d}u_{c\_\text{avg}}}{\text{d}t} \\ &= P_{\text{ac}} + NC_{c0}\frac{\text{d}u_{c\_\text{avg}}}{\text{d}t} + \frac{1}{2}NC_{\text{vir}}\frac{\text{d}u_{c\_\text{avg}}^2}{\text{d}t}. \end{aligned} \tag{4}$$

In (4), the differential component is easily disturbed by high-frequency signals. To eliminate the interference. The sampling point u_{c0_avg} after the delay T_s is introduced to replace the differential with the difference of the two sampling signals, and the SM capacitor voltage rating u_{c_ref} is added to modify the above formula to

$$\begin{aligned} \Delta P_{\text{vir}} &= \frac{1}{2}NC_{\text{vir}}\frac{\text{d}u_{c\_\text{avg}}^2}{\text{d}t} \\ &= \frac{1}{2T_s}NC_{\text{vir}}\left(u_{c\_\text{avg}}^2 - u_{c0\_\text{avg}}^2\right) \\ &= -\frac{1}{2T_s}C_{\text{vir}}\left[\left(u_{c\_\text{ref}}^2 - u_{c\_\text{avg}}^2\right) - \left(u_{c\_\text{ref}}^2 - u_{c0\_\text{avg}}^2\right)\right]. \end{aligned} \tag{5}$$

2) Control Strategy: Within the power outer loop, the active power is strongly coupled with the active current i_d. Therefore, convert the power increment into the active current increment $i_{d\text{vir}}$

$$i_{d\text{vir}} = 2\Delta P_{\text{vir}}/3v_{sd}. \tag{6}$$



(a) (b)

Fig. 3. SVCC. (a) Effect of SVCC on U_{dc}. (b) Limitation of adopting limiting control.

Based on (5) and (6), SVCC is designed, as shown in Fig. 1. Fig. 3(a) displays the dc voltage after incorporating the SVCC. During steady-state operation, the stator module voltage control ensures that $U_{c\_\mathrm{avg}} = U_{c\_\mathrm{ref}}$ and $i_{dvir} = 0$, resulting in the feed out of the SVCC. When a power disturbance occurs, $U_{c\_\mathrm{avg}} \neq U_{c\_\mathrm{ref}}$, and the inclusion of i_{dvir} causes a rapid change in the active current reference value, thereby reducing dc voltage oscillations during the power mutation process.

3) Strategy Optimization: Observing Fig. 3(a), it is evident that SVCC remains active throughout the entire power disturbance process. However, U_{dc} suffers from prolonged adjustment time due to the increased inertia. To address this issue, an adaptive limiting control is incorporated into the control scheme. When the capacitor voltage of the SM deviates from the set value U_{c_ref}, the SVCC is put into operation to reduce its oscillation amplitude. Subsequently, as the SM capacitor voltage approaches the reference value, the SM virtual inertia is forced to feed out to prevent it from hindering the recovery of the capacitor voltage.

The upper and lower bounds of the limiting controller are modified based on the average value of the SM capacitor voltage relative to its rated value, as shown in Fig. 3(b). Here, $i_{dv\mathrm{max}}$ and $i_{dv\mathrm{min}}$ denote the upper and lower limits. U_{ug} and U_{lg} represent startup thresholds.

During normal operation, U_{c_avg} may exhibit some ripples instead of being strictly fixed at the rated value. Therefore, while determining U_{ug} and U_{lg}, it is essential to incorporate a specific "dead zone" to ensure proper functionality. During this dead zone, when U_{c_avg} lies within the ripple range, both $i_{dv\mathrm{max}}$ and $i_{dv\mathrm{min}}$ are maintained at 0, and the SVCC remains inactive. This approach effectively prevents the interference of ripple with the control loop, allowing the control loop to circumvent the influence of the capacitor voltage ripple. The peak value of the capacitor voltage ripple defines the start-up thresholds, U_{ug} and U_{lg}. A comprehensive derivation of the capacitor ripple expression is presented in [24], and thus, this article refrains from delving into further details.

B. Virtual Inductance Control Strategy

1) Control Principle: The equivalent circuit of the dc side is shown in Fig. 4. This article focuses on bipolar short-circuit faults. When it occurred

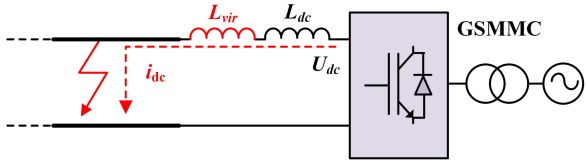


Fig. 4. DC side equivalent circuit.

$$U_{\mathrm{dc}} = i_{\mathrm{dc}} R_{\mathrm{dc}} + L_{\mathrm{dc}} \frac{\mathrm{d}i_{\mathrm{dc}}}{\mathrm{d}t} \tag{7}$$

where i_{dc} denotes the dc current and R_{dc} indicates the line equivalent resistance. Due to the small resistance of the dc line, the suppression effect on the current is restricted. Hence, we curb the current by increasing the equivalent line inductance L_{vir}

$$\begin{aligned} U_{\mathrm{dc}} &= i_{\mathrm{dc}} R_{\mathrm{dc}} + (L_{\mathrm{dc}} + L_{\mathrm{vir}}) \frac{\mathrm{d}i_{\mathrm{dc}}}{\mathrm{d}t} \\ &= i_{\mathrm{dc}} R_{\mathrm{dc}} + L_{\mathrm{dc}} \frac{\mathrm{d}i_{\mathrm{dc}}}{\mathrm{d}t} + \left(\frac{1}{2} L_{\mathrm{vir}} \frac{\mathrm{d}i_{\mathrm{dc}}^2}{\mathrm{d}t} \right) / i_{\mathrm{dc}}. \end{aligned} \tag{8}$$

In (8), the differential term is susceptible to high-frequency signals. Therefore, a similar approach as that of the virtual inertia of the previous SM is adopted. The above formula can be simplified to

$$\begin{aligned} \Delta U &= \left(\frac{1}{2} L_{\mathrm{vir}} \frac{\mathrm{d}i_{\mathrm{dc}}^2}{\mathrm{d}t} \right) \frac{1}{i_{\mathrm{dc}}} \\ &= \frac{1}{2T_s} L_{\mathrm{vir}} \left(i_{\mathrm{dc}}^2 - i_{\mathrm{dc0}}^2 \right) \frac{1}{i_{\mathrm{dc}}} \\ &= -\frac{1}{2T_s} L_{\mathrm{vir}} \left[\left(i_{\mathrm{dcref}}^2 - i_{\mathrm{dc}}^2 \right) - \left(i_{\mathrm{dcref}}^2 - i_{\mathrm{dc0}}^2 \right) \right] \frac{1}{i_{\mathrm{dc}}}. \end{aligned} \tag{9}$$

Here, T_s is the delay coefficient, i_{dc0} is the sampling value after delay, and i_{dcref} is the current steady-state rated value.

2) Control Strategy: The design of the dc control loop based on (9) is shown in Fig. 1. In steady state, $i_{\mathrm{dcref}} = i_{\mathrm{dc}}$, $\Delta U = 0$. In the initial stage of the fault, $i_{\mathrm{dcref}} < i_{\mathrm{dc}}$, $\Delta U > 0$, the VIC is put into operation, and the number of SM put into operation is reduced. As a consequence, the rise of the fault current is suppressed. When the line protection device transmits the fault ride-through signal, i_{dcref} switches to 0, leading to the direct current being reduced actively.

For grid-side HMMC, the converter station receives the active power transmitted by the offshore wind farm. Therefore, when a short-circuit fault occurs on the dc line, the transmission power of the wind farm is interrupted, and the current is first reduced to zero. After that, the SM capacitor and the ac line feed energy to the fault point, and the short-circuit current rises. The schematic diagram of the whole process is shown in Fig. 5(a).

IV. Transient Steady-State Cooperative Control

Based on the previous analysis, the ac and dc loops should optimize the transient stability characteristics under their specific working conditions, while avoiding adverse effects in other working conditions. Therefore, the collaborative analysis and

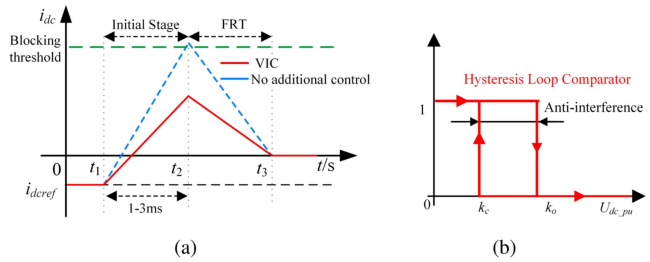


Fig. 5. Virtual inductance control. (a) Effect of VIC on i_{dc}. (b) Hysteresis loop comparator.

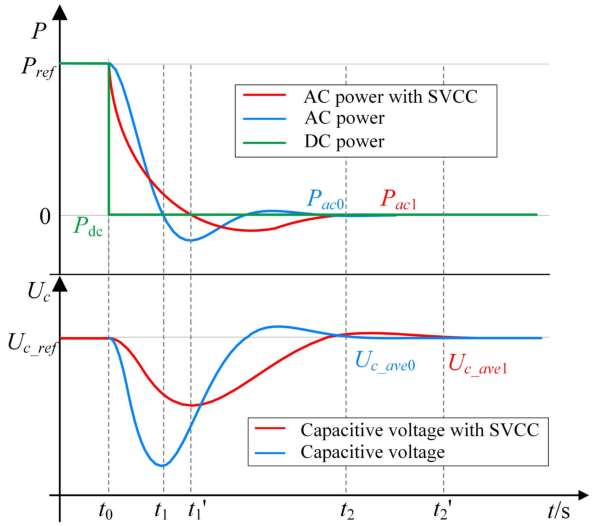


Fig. 6. Evolution of power and SM capacitor voltage under dc fault.

optimization of the ac and dc control loops under transient steady-state conditions are conducted. In the ac control loop, if no fault ride-through measures are taken during the fault phase, the energy stored in the SM virtual capacitor will continue to feed into the fault point, resulting in system instability. However, by adopting the fault ride-through strategy proposed in this article, the power evolution process of the converter station will change, as illustrated in Fig. 6.

In Fig. 6, a dc short-circuit fault occurs at time t_0. After detecting the fault, the converter station quickly reduces the number of SM, resulting in a rapid decrease of the dc power. The ac power is regulated by the PI controller with certain hysteresis and slow evolution speed. The energy difference will need to be supplemented by the SM capacitor, so that the voltage of the SM capacitor will drop. At time t_1, the ac power drops to 0, resulting in the largest power difference, and the deepest drop in SM capacitor voltage. In order to maintain the stability of the capacitor voltage of the SM, the converter will continue to adjust the active power until time t_2, when the SM capacitor voltage rises back to the rated value. It is not difficult to see from the whole process that under transient conditions, the power change process will make the evolution process of the SM capacitor voltage similar to the evolution process of the SM capacitor voltage under the steady-state disturbance in Fig. 3(a).

Therefore, adopting SVCC to respond to the change of the capacitor voltage of the SM can accelerate the decline of active power in the transient link. The P_{ac0} and U_{c_ave0} are evolved to P_{ac1} and U_{c_ave1}, respectively, while enhancing the inertia of the SM capacitor voltage. Therefore, SVCC can play a positive role in increasing the system inertia in the face of transient and steady-state conditions.

In the dc loop, the virtual inductance strengthens the coupling relationship between i_{dc} and U_{dc}. As long as the i_{dc} does not change continuously, the control loop will not cause malfunction due to sampling errors. At the same time, in order to prevent the false triggering of the control loop when the current changes are caused by the fluctuation of the source and load, a hysteresis loop comparison control is added on the outlet side of the VIC as the start criterion, which is shown in Fig. 5(b). When the dc voltage falls below k_c, the VIC initiates its operation, and when the dc voltage rises above k_o, the VIC is deactivated. In [25], it is demonstrated that the steady-state voltage reduction operation for the transmission line does not exceed 0.7 per unit (p.u.) To account for the sampling errors, k_c is configured as 0.69 p.u, providing a suitable threshold for VIC activation, while k_o is set at 0.71 p.u, ensuring VIC deactivation within the desired range. The structure makes it have certain anti-interference.

V. Stability Analysis

As the preceding analysis, C_{vir} and L_{vir} are the key parameters in the virtual inertial control loop. To investigate the impact of parameter variations on system stability, we establish small-signal models of both the ac and dc control loops.

A. Small Signal Modeling of AC Control Loop

To facilitate the analysis, the following two simplifications are made.

1) ΔU_c is replaced by ΔU_c^2.
2) The adaptive dynamic limiting control is ignored

The closed-loop transfer function between ΔU_d and ΔU_c^2 is established as follows:

$$G_1(s) = \frac{As^3 + Bs^2 + Cs + D}{(AH + T)\, s^3 + (BH + 1)\, s^2 + CHs + DH} \tag{10}$$

$$\begin{cases} A = k_{up}T_s k_{ip} + T_s M k_{ip} \\ B = k_{ui}T_s k_{ip} + k_{up}k_{ip} + k_{up}T_s k_{ii} + T_s M k_{ii} \\ C = k_{ui}T_s k_{ii} + k_{ui}k_{ii} + k_{ui}k_{ip} \\ D = k_{ui}k_{ii} \\ H = \frac{2i_{d0}}{NC} \\ M = \frac{NC_{\text{vir}}}{3T_s u_{d0}}. \end{cases} \tag{11}$$

Fig. 7 shows the locus of dominant eigenvalues when the virtual inertia parameter C_{vir} increases. System control and topology parameters are given in Table I.

The stability of the ac control loop is affected by C_{vir}. As C_{vir} increases, the closed-loop poles of the system move closer to the imaginary axis, reducing the stability margin. The increase in the inertia coefficient slows down the dynamic evolution process of the SM capacitor voltage. However, as C_{vir} continues to increase, the stability of the system weakens. Therefore, it is

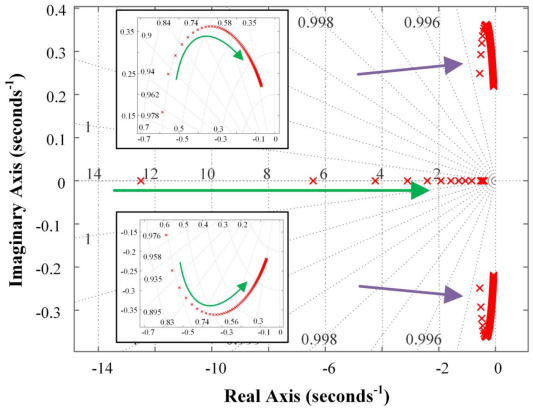


Fig. 7. Zeros and dominant poles distribution. Arrow direction: C_{vir} changing from 0.1 to 50.

TABLE I
ELECTRICAL SYSTEM PARAMETERS

Component	Parameter	Value
Transmission line	DC reactor	$L_{\text{dc}} = 200$ mH
	Rated voltage	$U_{\text{dc}} = 400$ kV
Transformer	Turn ratio	$K = 230/210$
MMC	Rated SM voltage	$U_{\text{c\_avg}} = 2$ kV
	Rated voltage	$U_{\text{dc}} = 400$ kV
	HBSM count	200
	FBSM count	200
	Arm inductance	$L_{\text{arm}} = 76$ mH
	Real power	$P_{\text{ref}} = 400$ MW
SVCC	Time constant	$T_s = 0.05$ s
	virtual capacitance	$C_{\text{vir}} = 3$ mF
VIC	Time constant	$T_s = 0.05$ s
	Virtual inductance	$L_{\text{vir}} = 0.3$ H
Voltage outer loop	Proportional coefficient	$k_{up} = 2$
	Integral coefficient	$k_{ui} = 0.04$
Current inner loop	Proportional coefficient	$k_{ip} = 10$
	Integral coefficient	$k_{ii} = 0.01$

recommended to choose a value of C_{vir} within the interval with a large stability margin. Based on the actual parameters in this study, a value of $C_{\text{vir}} = 3$ mF is suggested.

B. Small Signal Modeling of DC Control Loops

According to Fig. 1, the closed-loop transfer function whose input is Δi_{dc}^2 and output is ΔM is constructed as follows,where $K_1 = L_{\text{vir}}/2Ti_{\text{dc0}}, K_2 = 2u_{c0}i_{\text{dc0}}/L_{\text{dc}}$:

$$G_2(s) = \frac{L_{\text{vir}}L_{\text{dc}}s}{(2L_{\text{vir}}u_{c0}i_{\text{dc0}} + 2TL_{\text{dc}}i_{\text{dc0}})\,s + 2L_{\text{dc}}i_{\text{dc0}}}. \quad (12)$$

The transfer function of the virtual inductor-based dc control loop is a first-order system with all positive parameters, which means that the closed-loop zero and pole points are located on the left side of the imaginary axis, ensuring the stability of the

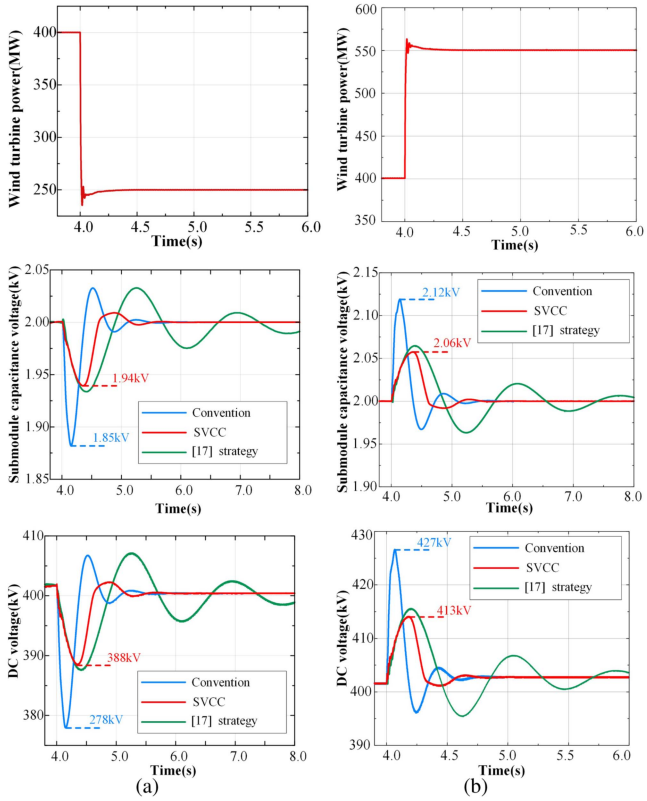


Fig. 8. Simulation results of wind field output disturbance. (a) DC power decrease. (b) DC power increase.

control loop. Increasing L_{vir} can better limit the rise of short-circuit current, but it may also lead to a significant drop in dc voltage and result in transmission power interruption. Therefore, there is a tradeoff between limiting fault current and mitigating power interruptions.

VI. SIMULATION VERIFICATION

To verify the proposed resilience enhancement strategy, an offshore wind power transmission system, as shown in Fig. 1, was built in PSCAD/EMTDC. The simulation results are compared with the virtual capacitor control adopted in [16] and the dc voltage feedforward control adopted in [23]. The key parameters of the whole system are given in Table I.

A. DC Power Fluctuation

The wind farm power disturbance is designed, including dc load increase and dc load decrease.

Fig. 8(a) shows the simulation results of the dc power decrease. At 4 s, the active power output of the wind farm is reduced to 250 MW. With a small dc power grid inertia, the dc voltage changes drastically, resulting in poor power quality, and the voltage drop depth exceeds 20 kV. With the adoption of SVCC, the converter quickly releases the auxiliary power in response to external signals, providing virtual inertia support. This suppresses the fluctuation of the dc and SM capacitor voltages, and reduces the depth of the voltage drop to half of

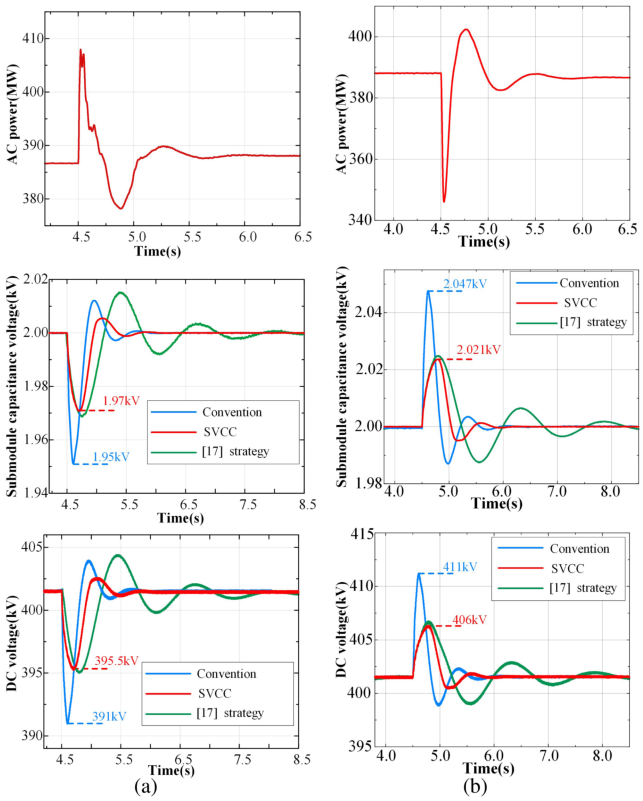


Fig. 9. Simulation results of ac power disturbance. (a) AC power decrease. (b) AC power increase.

the original value. In addition, due to the implementation of the adaptive limiting control, compared with the virtual capacitance control, SVCC does not increase the adjustment time of the whole process.

Fig. 8(b) shows the simulation results of the dc power increase. At 4 s, the active power output of the wind farm rises to 550 MW. This power difference directly impacts the SM, leading to an increase of 0.12 kV in the SM capacitor voltage and 25 kV in the dc voltage. With the presence of SVCC, the inertia of both the SM capacitor voltage and dc voltage is strengthened. Consequently, under the same power disturbance, the SM capacitor voltage exhibits a smaller increase of 0.06 kV, whereas the dc voltage only rises by 12 kV. In addition, the adaptive dynamic limiting component, incorporated within SVCC, ensures that the adjustment time of the system remains unaffected compared with the control strategy proposed in [16].

B. AC Power Fluctuation

The ac gird power disturbances are designed, including ac load increase and ac load decrease.

Fig. 9(a) shows the simulation results of ac power increase. At 4.5 s, the ac power undergoes a sudden 20 MW increase, followed by a return to the rated value. With the inclusion of SVCC, the depth of the SM capacitor voltage drop is reduced from 0.05 kV to 0.03 kV, and the depth of dc voltage drop is reduced from 9 kV to 4.5 kV. Importantly, these improvements

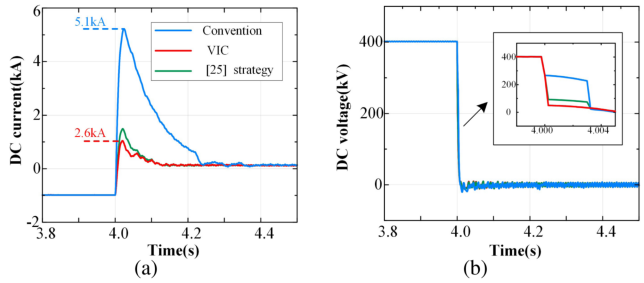


Fig. 10. Simulation results for dc faults. (a) DC current. (b) DC voltage.

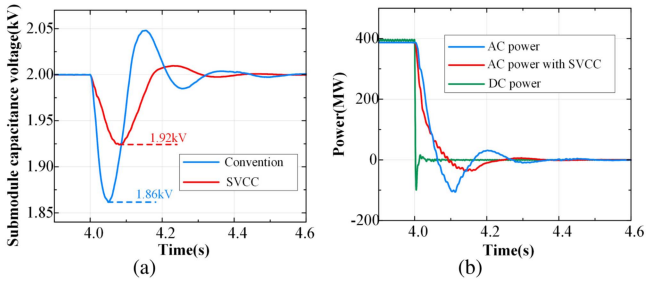


Fig. 11. Simulation results for dc faults. (a) SM capacitance voltage. (b) Power.

in voltage stability are achieved without any extension of the adjustment time.

Fig. 9(b) illustrates the simulation results of the ac power decrease. At 4.5 s, the ac power experiences a sudden drop of 40 MW, followed by a recovery to the rated value. With the integration of SVCC, the rise height of the SM capacitor voltage is reduced from 0.047 kV to 0.021 kV, and the rise height of the dc voltage is reduced from 10 kV to 5 kV. Notably, these voltage stabilization enhancements are achieved without any extension of the adjustment time.

C. DC Fault

To verify the effect of VIC, a short-circuit fault on the dc side is designed. At 4 s, a bipolar short-circuit fault occurs on the dc side. With a control delay of 600 μs, VIC was put to work. After 3 ms, the line protection device detects the fault and sends a fault ride-through signal. I_{dcref} switches to 0, and the dc current is actively reduced.

Fig. 10 shows the simulation results. When the fault occurs, the quick input of VIC makes the dc voltage decrease rapidly, suppressing the rise of i_{dc} from 5.1 kA to 2.6 kA. The dc voltage is quickly reduced to 100 kV. It can be seen that the dc voltage feed-forward control will also cause the dc current to rise slowly, but its problem will be stated in the next section.

D. Transient Steady State Cooperative Strategy

To verify the superiority of the control strategy in the transient and steady state, Fig. 11 shows the response results of SVCC under dc fault.

After a short-circuit fault occurs on the dc side, the input of VIC makes the dc power drops rapidly, and the ac power

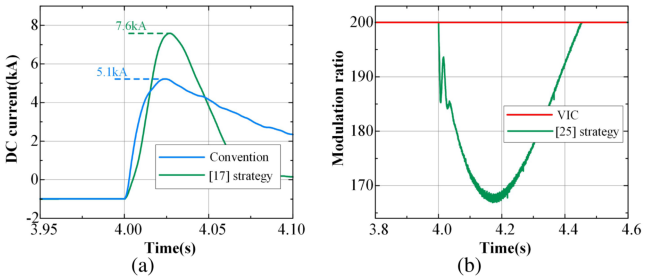


Fig. 12. Control effect comparison with [16] and [23]. (a) DC current. (b) Modulation ratio.

drops slowly under the regulation of the PI control loop. The power difference causes the SM capacitor voltage to oscillate. The SVCC accelerates the decline of active power, providing inertial power support for the SM capacitor and reducing the depth of SM capacitor voltage drop from 1.86 to 1.93 kV. The whole process proves that the SVCC also has certain advantages in the transient state.

Fig. 12(a) shows the response result of the virtual capacitor control strategy under dc faults. It can be observed that when the dc voltage drops, the virtual capacitor will continue to inject active power into the fault point in response to the change of dc voltage and accelerate the rise of dc current.

Fig. 12(b) shows the dc modulation ratio of dc voltage feedforward control and VIC during power disturbance. It can be seen that the virtual capacitor does not malfunction under steady-state conditions, but the dc voltage feedforward control will actively reduce the dc modulation ratio, which have an adverse effect on the stable operation of the power grid.

In summary, a comprehensive analysis of Figs. 8, 9, and 12 reveal the significant role played by the SVCC in enhancing the inertia of dc voltage, resulting in improved transient and steady-state performance. In addition, Figs. 10 and 12 demonstrate that the VIC effectively suppresses the initial rising speed of the short-circuit current. Notably, VIC demonstrates robustness and avoids malfunction even when subjected to steady-state load power fluctuations.

VII. Experimental Result

To verify the performance of the proposed control strategy, the experimental setups shown in Fig. 13 are built. Including Rtunit-HMMC-024 converter, ac grid simulator ITECH-350, controller Rtbox, and control computer. In the whole system, MMC works in the rectifier mode. The key parameters of the system are given in Table II.

A. DC Power Fluctuation

Fig. 14 shows the results when the load resistance is switched from 100 Ω to 50 Ω. It can be seen that the SM capacitor voltage and dc voltage exhibit a 50% reduction in the depth of the voltage drop. Furthermore, due to the adaptive limiting control, the adjustment time of the system does not increase significantly.

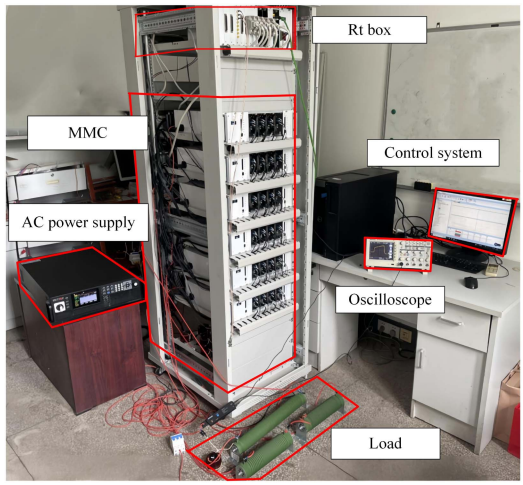
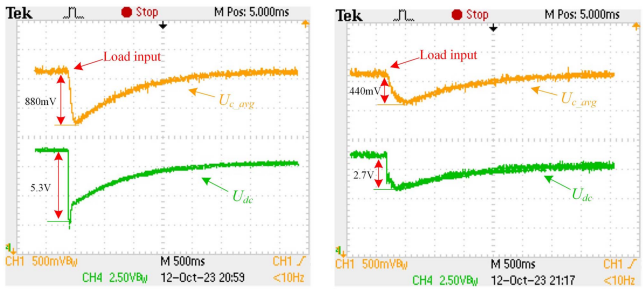


Fig. 13. Laboratory setups.

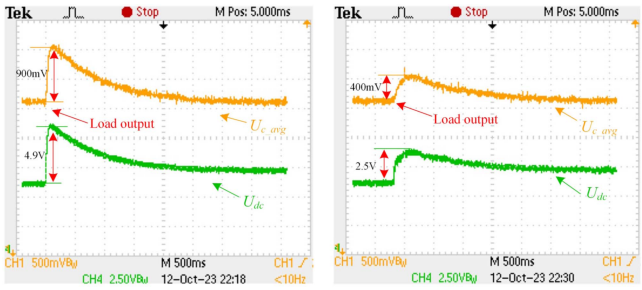
TABLE II
Experimental Parameters

Component	Parameter	Value
DC load	DC resistance	$R = 100\omega$
	DC reactor	$L_{\mathrm{dc}} = 2.5$ mH
AC source	AC voltage	$U_{\mathrm{ac}} = 50$ V
	AC inductance	$L_{\mathrm{ac}} = 2.5$ mH
MMC	SM rated voltage	$U_{\mathrm{c\_avg}} = 25$ V
	SM Capacitance	$C_c = 2.7$ mF
	FBSM count	4
	Arm inductance	$L_{\mathrm{arm}} = 5$ mH
SVCC	Time constant	$T_s = 0.05$ s
	virtual capacitance	$C_{\mathrm{vir}} = 3$ mF
VIC	Time constant	$T_s = 0.05$ s
	Virtual inductance	$L_{\mathrm{vir}} = 0.01$ H
Voltage outer loop	Proportional coefficient	$k_{up} = 2$
	Integral coefficient	$k_{ui} = 0.3$
Current inner loop	Proportional coefficient	$k_{ip} = 4$
	Integral coefficient	$k_{ii} = 0.1$



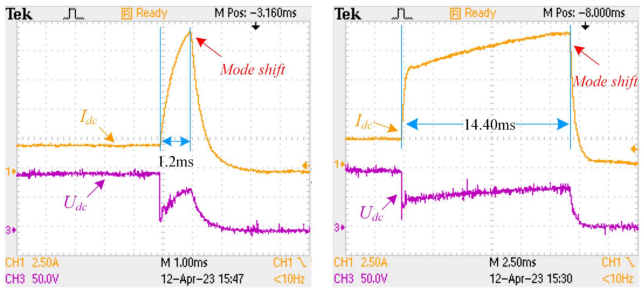
(a) (b)

Fig. 14. Experimental waveforms of dc load increases. (a) With traditional control. (b) With SVCC.



(a) (b)

Fig. 15. Experimental waveforms of dc load decreases. (a) With traditional control. (b) With SVCC.



(a) (b)

Fig. 16. Experimental waveforms for dc fault. (a) With traditional control. (b) With VIC.

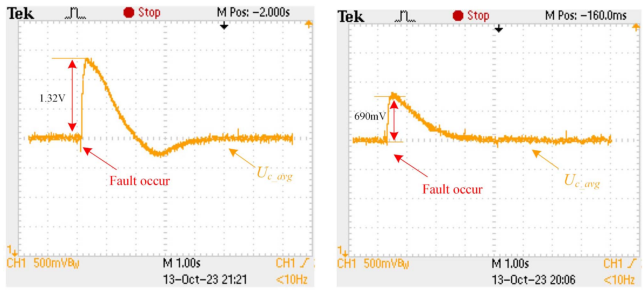
Fig. 15 shows the results when the load resistance is switched from 50 Ω to 100 Ω. The SM capacitor voltage and dc voltage increase by 900 mV and 4.9 V, respectively. However, with SVCC, the elevation in SM capacitor voltage and dc voltage is reduced to 400 mV and 2.5 V, respectively.

B. DC Fault

Fig. 16 shows the dc current when a dc fault occurs. We demonstrate the effectiveness of the control strategy by comparing the time to reach the threshold. When the dc current is less than 5 A, it is regarded as the initial stage of the fault. After reaching the peak, the controller switches to constant current fault ride-through, and I_{dcref} is set to 0.

As depicted in Fig. 16, there exists a control delay of 700 μs, during which the rise of the short-circuit current occurs without any influence from the controller. Then, the virtual inductance is activated. This results in a significant reduction in the current rise speed, and the time required to reach the threshold is reduced from 1.2 to 14.4 ms. These findings highlight the effectiveness of the control strategy in reducing the current rise.

Fig. 17 illustrates the waveform of the SM capacitor voltage during a dc fault event. As a result of the implemented ride-through strategy, the SM capacitor voltage begins to ascend. With the intervention of the SVCC, the active power of the ac power grid experiences an accelerated decline, leading to a reduction in the peak voltage rise of the capacitor from 1.32 V to 690 mV.



(a) (b)

Fig. 17. Experimental waveforms for dc fault. (a) With traditional control. (b) With SVCC.

VIII. Conclusion

This article proposed a resilience enhancement strategy based on HMMC for the offshore wind power transmission system, including the dc voltage inertia enhancement strategy based on SM virtual inertia control and the ride-through control strategy based on virtual inductance. The effectiveness of the proposed control strategy was verified on the simulation and experimental platform, and the specific conclusions were as follows.

1) The SVCC adjusted the virtual power by responding to changes in the SM capacitor voltage, thereby providing support for the dc voltage during load fluctuations.
2) The VIC strategy adjusted the dc modulation ratio by responding to changes in dc current. In the event of a short-circuit fault on the line, the VIC strategy promptly activated without waiting for the protection device's action signal, effectively limiting the rise in fault current.
3) The cooperation of the two control methods enabled the SVCC to play a positive role in dc faults. The inclusion of a hysteresis comparator ensured that the virtual inductor was not falsely triggered during normal operation.

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